REMARKS/ARGUMENTS

Claims 27-52 are pending in the application. Claims 27-28, 31, 36, 38-39, 42-43, 47, 49, and 51-52 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Missing Reference

In the office action dated 09/24/04, the Examiner first relied on U.S. Patent No. 4,862,452 (Milton et al.) to reject claims. However, that reference was not listed on the PTO-892 Form that accompanied that office action. The reference does not appear to have been formally acknowledged by the Examiner. The Applicant hereby requests that the Examiner list the reference on a PTO-892 Form in order to formally acknowledge the reference.

Prior-Art Rejections

On page 2 of the office action, the Examiner rejected claims 27-30 and 33-51 under 35 U.S.C. 102(b) as being anticipated by Milton. On page 5, the Examiner rejected claims 31-32 and 52 under 35 U.S.C. 103(a) as being unpatentable over Milton in view of Brown. For the following reasons, the Applicant submits that all of the non-pending claims are allowable.

Improper Grounds for Rejection

Claim 32 was rejected under 35 U.S.C. 103(a). Claim 33, which depends from claim 32, was rejected under 35 U.S.C. 102(b). As such, the Applicant submits that the rejection of claim 33 under 35 U.S.C. 102(b) is improper.

Claims 27, 38, 49, and 51

Claim 27 has been amended to clarify that the data signal is converted, in the signal unit, into one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal. For example, in the exemplary embodiment described in the specification, the data signal is analyzed to determine which data bits have a logic ONE value, where a different interrupt signal is generated for each different analyzed data bit having a logic ONE value.

(Note that, in other embodiments of claim 27, the specified bit value could be a logic ZERO value, instead of a logic ONE value. Moreover, not every bit in the data signal need be analyzed. For example, in possible embodiments, fewer than all eight (e.g., only seven) of the bits in an 8-bit data signal might be used in the interrupt signal processing of the invention, where one or more bits in the data signal are unused.)

None of the cited references teaches the combination of features recited in currently amended claim 27.

In particular, Milton does not teach a signal unit that analyzes the bit values of one or more data bits in a data signal in order to convert the data signal into one or more interrupt signals, where each analyzed data bit having a specified bit value corresponds to a different interrupt signal.

In rejecting previously pending claim 31, the Examiner admitted that "Milton fails to explicitly teach wherein the signal unit **detects** a transition in each data bit of the data signal over time to determine when to generate a corresponding interrupt signal." Instead, the Examiner cited Brown as providing the teachings missing from Milton. For the following reasons, the Applicant submits that the Examiner misapplied the teachings in Brown in rejecting previously pending claim 31.

The passages in Brown cited by the Examiner relate to the processing of an interrupt request signal by the recipient of that already existing signal. In particular, the recipient of an interrupt request signal has an edge detector that "detects a 0 to 1 transition of the interrupt request signal." See column 30, lines 19-20. The passages in Brown cited by the Examiner do not teach anything about how the interrupt request signal is generated, only how an already generated interrupt request signal is processed by the recipient of that signal.

The present invention, on the other hand, relates to the generation of one or more interrupt signals from a data signal. According to currently amended claim 27, a signal unit converts the data signal into the one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal. Significantly, in the present invention, the recited features relate to the analysis of the bit values in the data signal that is converted into one or more interrupt signals. This differs from Brown, where the value of an already existing interrupt request signal is analyzed.

Since the cited teachings in Brown have nothing to do with generation of an interrupt signal, the Applicant submits that the teachings in Brown have been misapplied in rejecting previously pending claim 31. For similar reasons, the Applicant submits that currently amended claim 27 is allowable over the cited references. Likewise, the Applicant submits that currently amended claims 38, 49, and 51 are also allowable over the cited references. Since claims 28-37, 39-48, 50, and 52 depend variously from claims 27, 38, 49, and 51, it is further submitted that those claims are also allowable over the cited references.

Claims 29, 40, and 52

According to claims 29, 40, and 52, at least two interrupt signals are transmitted to two different interrupt ports of a single other processor. In rejecting claim 29, the Examiner stated that Milton teaches this feature, citing column 2, lines 21-63, and column 1, lines 58-68. The Applicant submits that, in fact, Milton does not teach, either in the cited passages or anywhere else, that at least two interrupt signals are transmitted to two different interrupt ports of a single other processor. In particular, each DSP module 13 in Milton's Fig. 1 is depicted with a single interrupt port connected to receive a single interrupt signal from main controller 1. The Applicant submits that this provides additional reasons for the allowability of claims 29, 40, and 52 over the cited references.

Claims 33 and 44

According to claims 33 and 44, the first processor transmits an address signal to the signal unit, where the signal unit compares the address signal to a specified value to determine whether to store the two sequential values in the two registers. In rejecting claim 33, the Examiner stated that Milton teaches this feature, citing column 1, lines 58-68, and column 4, lines 44-55. The Applicant submits that, in fact, Milton does not teach, either in the cited passages or anywhere else, that a first processor transmits an address signal to a signal unit that compares the address signal to a specified value to determine whether to store the two sequential values in the two registers. In particular, neither column 1, lines 58-68, nor column 4, lines 44-55, teaches anything about a signal unit comparing an address signal to a specified value to determine whether to store two sequential values of a data signal in two registers. The

Applicant submits that this provides additional reasons for the allowability of claims 33 and 44 over the cited references.

Claims 36 and 47

Claims 36 and 47 recite an "other signal unit" (i.e., different from the "signal unit" previously recited in claims 27 and 38). In rejecting claim 36, the Examiner stated that Milton teaches the features recited in that claim, stating that "Milton teaches switching and bidirectional communication of DSP modules." The Applicant submits that, just because Milton might teach "switching and bidirectional communication of DSP modules" (which the Applicant does not necessarily admit), that does not mean that Milton teaches two different signal units operating on conjunction with those DSP modules.

According to the Examiner, DSP modules 13 of Milton's Fig. 1 are examples of the first processor an one or more other processors of claim 27. Although the Examiner does not explicitly say so, presumably, the Examiner believes that Milton's main controller 1 is an example of the signal unit of claim 27. Significantly, Milton does not teach more than just that one main controller receiving and transmitting interrupt signals from and to the DSP modules. As such, Milton does not teach or even suggest an example of the "other signal unit" recited in claims 36 and 47. The Applicant submits that this provides additional reasons for the allowability of claims 36 and 47 (and therefore claims 37 and 48) over the cited references.

For all these reasons, the Applicant submits that the rejections of claims under 35 U.S.C. 102(b) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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